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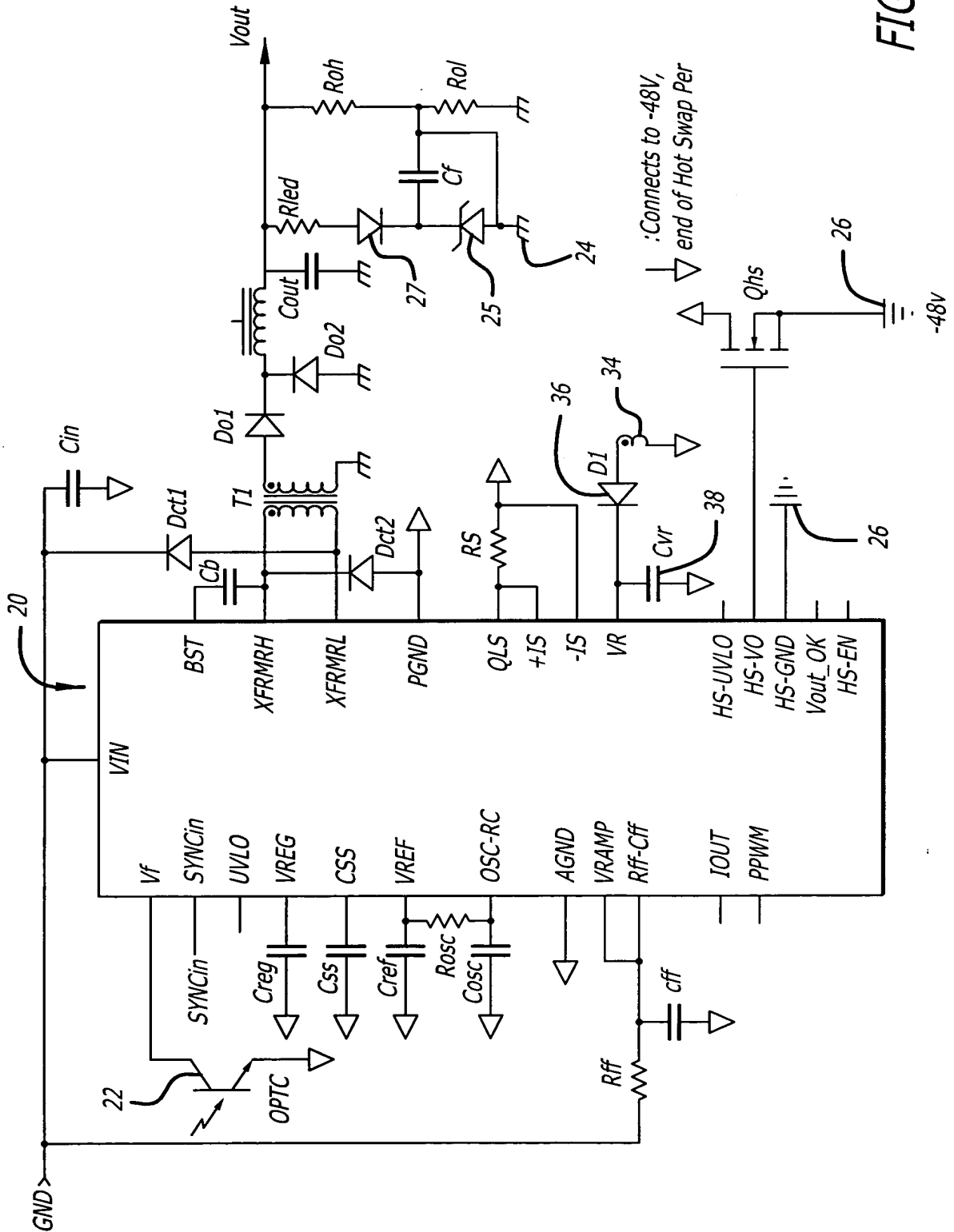


FIG. 1

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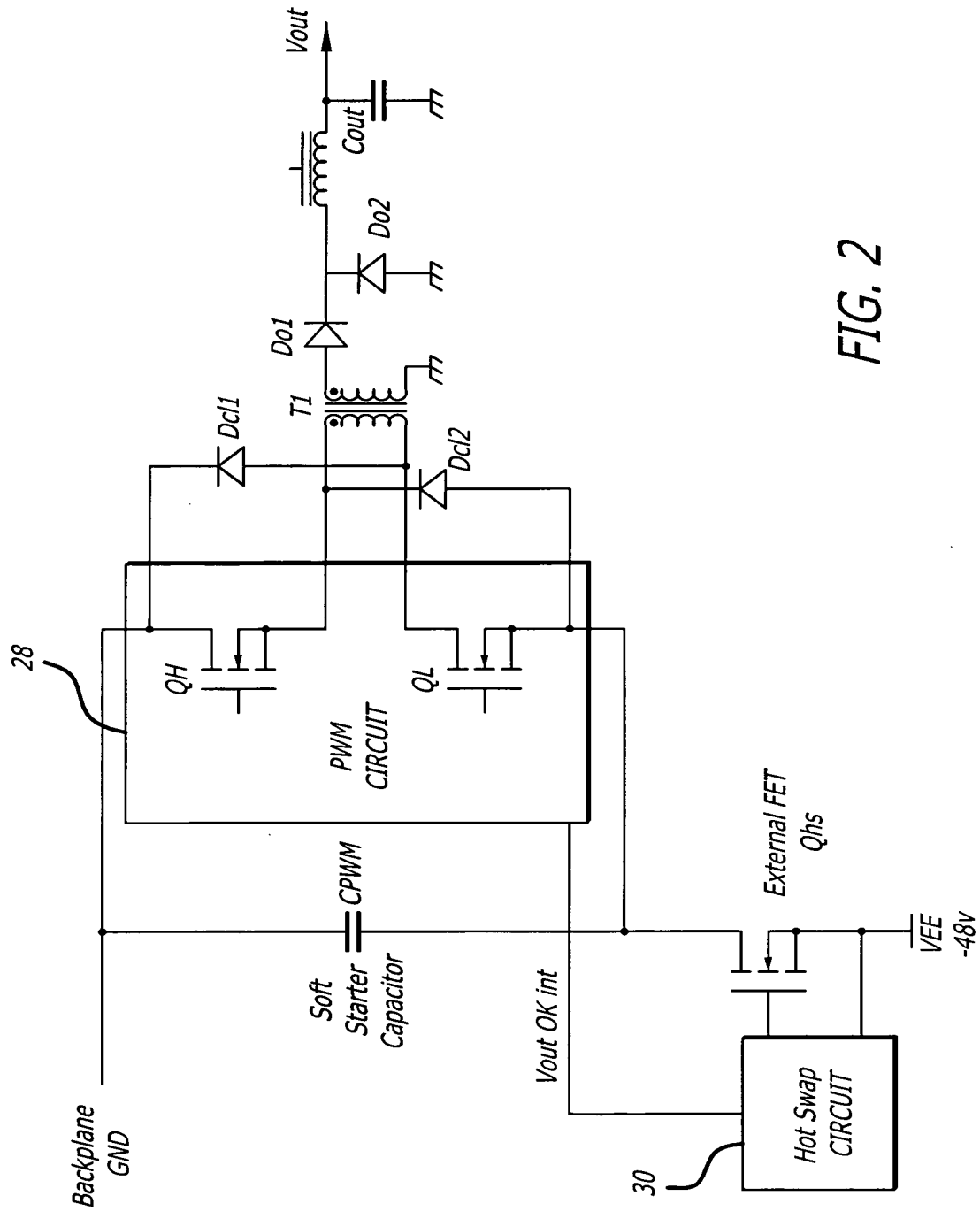
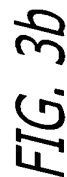


FIG. 2

FIG. 3a

The diagram illustrates a power MOSFET driver circuit with various protection features. Key components include:

- Input Stage:** VIN is connected to a network of resistors (24*R1, R1) and capacitors (CFF, Ramp, Vrpp) leading to a VREF input. A VREF pin is also present.
- Control Logic:** A PWM input is connected to a Vref pin, which feeds into a REF-CONP comparator. The output of REF-CONP is Vref_good, which is ANDed with a Vreg_good signal (from a Vreg-CONP comparator) to produce a 32-bit signal. This signal is connected to the HV Start pin (42) of the VR Regulator.
- VR Regulator:** The VR Regulator (44) has a feedback loop with a VR pin and a CVR pin. Its output is connected to the gate of the QH MOSFET.
- Thermal Shutdown:** A Global Thermal Shutdown block (52) receives a Thermal Shutdown Powered From Vin signal (54) and outputs a Global Shutdown signal (50).
- Current Limiting:** A current sense resistor (R1) is placed in the source path of the QH MOSFET. The voltage across it is sensed by a UVLO (Under Voltage Lock Out) block (70), which outputs a UVLO signal (72). This signal is connected to a T_FF (Threshold Flip-Flop) block (72).
- Output Stage:** The QH MOSFET is connected to the load (XFRMRH) and the source is connected to the output (IOUT). The drain is connected to the load and the source is connected to the output.
- Protection Features:** A Vout-OK_int signal (50) is connected to a Global Shutdown block (52). A Vout-OK_int signal (50) is also connected to a Global Shutdown block (52).
- Timing and Frequency:** An OSC block (70) is connected to the clock (clk) input of the T_FF block (72). A VAMP block (70) is connected to the VAMP input of the T_FF block (72).
- Current Limiting:** A current sense resistor (R1) is placed in the source path of the QH MOSFET. The voltage across it is sensed by a UVLO (Under Voltage Lock Out) block (70), which outputs a UVLO signal (72). This signal is connected to a T_FF (Threshold Flip-Flop) block (72).
- Current Limiting:** A current sense resistor (R1) is placed in the source path of the QH MOSFET. The voltage across it is sensed by a UVLO (Under Voltage Lock Out) block (70), which outputs a UVLO signal (72). This signal is connected to a T_FF (Threshold Flip-Flop) block (72).



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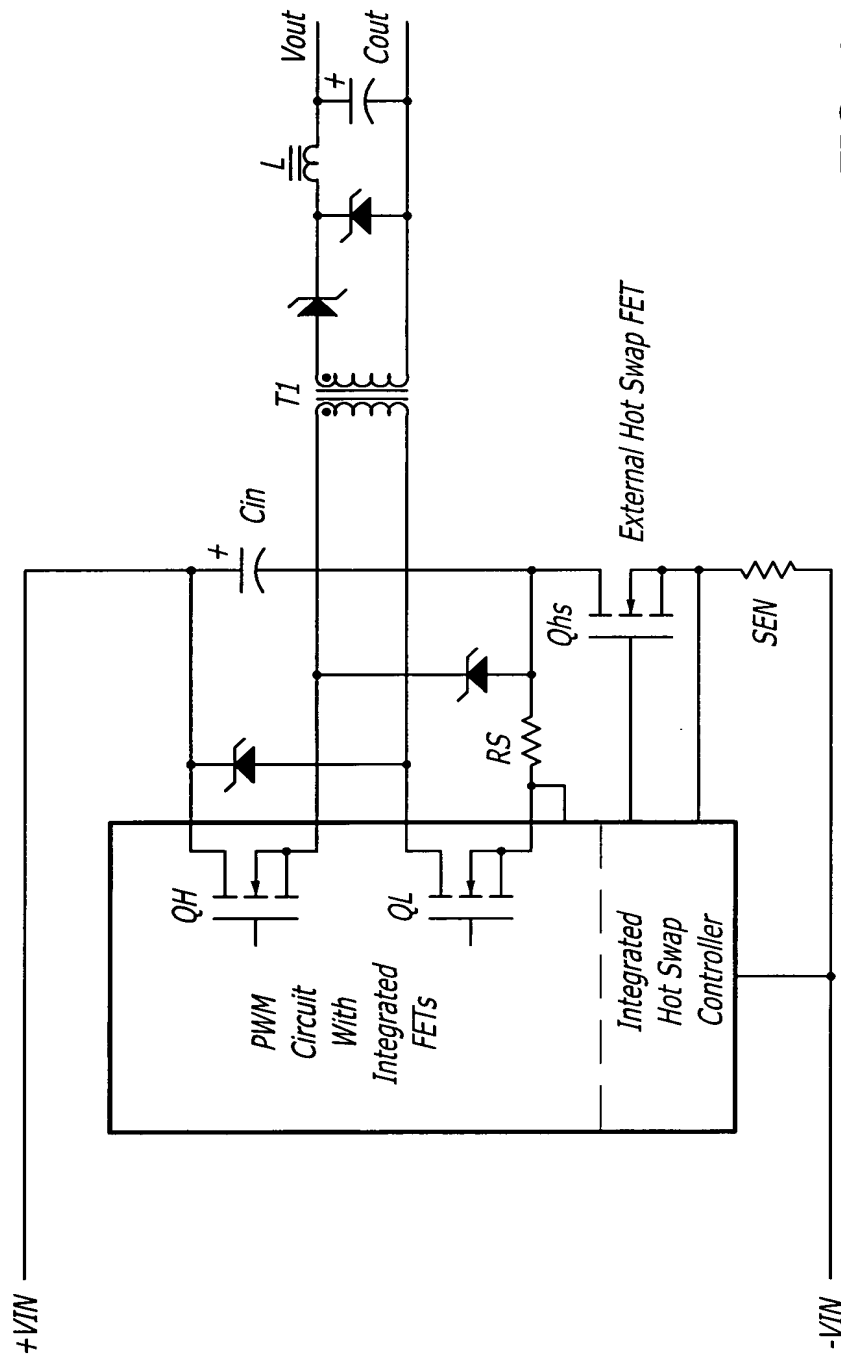


FIG. 4